REMARKS

In the interest of clarity, the Item Numbers below correspond to the Examiner's Item Numbers in the Office Action.

1. Claims 1-75 were pending. However, responsive to the 10/21/02 Restriction Requirement and the 11/14/02 Response thereto, Applicant hereby cancels Claims 31-33 and 35-75 without prejudice or disclaimer, and with traverse, by which **Claims 1-30 and 34 are currently pending**, and which Applicant will presently discuss.

2. The Examiner objected to Fig. 6 because the decision block 80d has only one output, i.e., the Examiner believed it should have two outputs, YES and NO. Respectfully, Applicant traverses and requests withdrawal.

Applicant respectfully acknowledges that some traditional decision blocks have two outputs. However, throughout the Specification, Applicant maintains that only one of four output signal combinations is possible. For example, referring to Fig. 2, Applicant notes that each flip-flop 62 and 64 respectfully outputs a signal 34 and 32 with a logical 1 or a logical 0 thereon. *See, e.g., Page 7, lines 11-12.* As understood by one skilled in the art, the two signal branches 32, 34 must therefore yield one of a maximum of four possible combinations, namely (0,0), (0,1), (1,0), or (1,1), which Applicant made explicit in Fig. 5. *See Fig. 5.* More explicitly, Applicant notes, in describing Fig. 5, that "four possible combinations of the logic levels of PH1 signal 32 and PH2 signal 34 are illustrated." *Page 8, lines 23-24.* Accordingly, in referring to Fig. 6, it is understood that one of the four conditions (i.e., Conditions 1-4 (84a-84d)) must exist, whereby if none of Conditions 1-3 are true, then Condition 4 must true. *See, e.g., Page 10, lines 25-27.*

Moreover, as is manifest from the entirety of Applicant's description, the order of checking which of the four conditions is presently true is insignificant—**any order can be used**. Applicant made this explicit when originally describing Fig. 6, to wit, "This leads to a series of four decisions 80A through 80D...Although the series of decisions are shown made in **a** serial fashion...these operations could also be arranged to run in parallel, so long as the determinations are made." *Page 10, lines 11-14 (emphasis added).* More notably, Applicant noted that the decisions were shown in "a" representative serial fashion, whereby other serial fashions were also contemplated and disclosed, as well as possibly arranging for parallel processing.

Accordingly, as noted above, Applicant has amended this part of the description of Fig. 6 to make explicit that which was implicit, namely that other serial arrangements (other than that depicted in Fig. 6) are—and always were—contemplated, to wit, "This leads to a series of four decisions ~~80A through 80D~~ 80a through 80d...Although the series of decisions are shown made in a serial fashion...these operations could also be rearranged to run in other serial fashions or in parallel, so long as the determinations are made."

As a result of the foregoing, applicant depicted 80d in Fig. 6 as a traditional decision node because, whereas while it must always be true in the represented depiction (i.e., since it is the last decision node in the serially checked series), it otherwise functions as a traditional decision node if it is otherwise examined prior to being the last checked node, whereby a NO would lead to checking one of the other four conditions, the last decision node always defaulting to a true condition with serial processing without the need for it to function as a traditional decision node, whereas Applicant, intending to depict the serial nodes as **fully interchangeable units**, thus depicted 80d as a traditional decision node in so far as it is fully interchangeable with the other serial decision nodes. Because their order is irrelevant, however, each of the following series of process steps, taken in their entirety, can be substituted for any of the others in any order: [80a, 82a, and 84a], [80b, 82b, and 84b], [80c, 82c, and 84c], and [80d, 82d, and 84d], whereas a NO at any one of them leads to checking the others, whereby at least one must always be true, and if the first three conditions are not true, then a final condition must always, therefore, be true.

In other words, Applicant has made clear that one of the four decisions must be true, whereby if condition 1 is not satisfied 81, and condition 2 is not satisfied 83, and condition 3 is not satisfied 85, then one skilled in the art would recognize that condition 4 must be satisfied, for which it would not be necessary to depict a NO output. Applicant has properly shown it as a traditional decision block because the condition checking steps (i.e., Conditions 1-4 (84a-d)) can be performed in any order (or in parallel), in which case a NO at 80d would require checking one of the other conditions when arranged in a different serial arrangement, the checking continuing until the one true condition is reached, or the last condition being automatically true by default, but not necessarily so if said condition was not the terminal condition.

If necessary, Applicant hereby encourages the Examiner to telephone the undersigned attorney to discuss the foregoing. Otherwise, earnestly believing that Fig. 6 complies with all

applicable requirements, Applicant respectfully requests reconsideration and allowance of the same.

3-4. The Examiner objected to the Abstract of Disclosure for improper language and format. Respectfully, Applicant traverses and requests withdrawal. However, as requested, and in compliance with M.P.E.P. § 608.01(b), Applicant amended the Abstract to eliminate the implied phrase "is disclosed." Applicant also made other minor, non-substantive, editorial changes so that the Abstract would be within a requested 50-150 word range. Earnestly believing the Abstract now contains proper language and format, Applicant respectfully requests reconsideration and allowance of the same.

5. The Examiner objected to the Specification for failing to provide proper antecedent basis for the claimed subject matter. Respectfully, Applicant traverses and requests withdrawal.

The Examiner indicates that the Examiner did not see the phrase "measurement delay line" in the Specification, to which Applicant respectfully directs the Examiner to Page 6, lines 12-13 for explicit reference to this precise language: "As is known in the art, the SMD 12 includes a **measurement delay line**...". *Page 6, lines 12-13 (emphasis added).* In addition, as elaborated upon below in conjunction with Item Number 6, Applicant respectfully directs the Examiner to Page 6, line 15 for explicit reference to the phrase variable delay line: "The **variable delay line** is also a plurality of serially connected delay elements..."). *Page 6, line 15.*

Moreover, Applicant also explicitly references an "**output** of the measurement delay line" and an "**output** of the variable delay line," *Page 6, lines 14-16 (emphasis added)*, respectively providing explicit support for the terms "**measurement delay line output**" and "**variable delay line output**" as recited in Claim 19, but the former being claimed as not seen by the Examiner, whereas now the Examiner may see it. Finally, Applicant also explicitly references "the **input** to a variable delay line," *Page 6, lines 14-15 (emphasis added)*, providing explicit support for the term "**variable delay line input**" as recited in Claim 19, but claimed as not seen by the Examiner, whereas now the Examiner may see it.

Notwithstanding the foregoing, the "measurement delay line" and "variable delay line" of the SMD 12, as understood by one skilled in the art, each have an input and an output, thereby providing the "**measurement delay line input**," "**measurement delay line output**," "**variable delay line input**," and "**variable delay line output**," as referenced in Claim 19. Nevertheless, Applicant amended the Specification on Page 6, lines 13, 16 to make explicit that which was

implicit, namely, that the measurement delay line has a **measurement delay line input** and **measurement delay line output**, and that the variable delay line has a **variable delay line input** and **variable delay line output**, as would have been—and is—understood by one skilled in the art. As noted above, Applicant has provided ample support for this amendment throughout the Specification. *See, e.g., Page 2, lines 16-17* ("For the conventional SMD implementations, two delay lines are required, one for delay measurement, one for variable mirrored delay"); *Page 2, line 21* ("the delay stages required for each delay line..."); *Page 3, line 4* ("For two delay lines in ~~an~~ a SMD..."), *and Page 11, lines 9 and 19-20* ("delay line 128").

The Examiner may now explicitly see that which was explicit and implicit, namely that Applicant described each of the terms used in Claim 19 in the Specification. Earnestly believing that the Specification does not—and did not—fail to provide proper antecedent basis for the claimed subject matter, Applicant respectfully requests reconsideration and allowance of the same.

6. The Examiner rejected Claims 19-22 and 26-30 under 35 U.S.C. § 112, ¶2 as being indefinite for failing to particularly point out and distinctively claim the subject matter which Applicant regards as the invention. Respectfully, Applicant traverses and requests withdrawal.

Regarding **Claim 19, lines 2-4**, the Examiner asserts that the recitation is misdescriptive. However, Applicant respectfully directs the Examiner to the following description of Fig. 1:

> An external clock signal 16 is input into receiver and buffer 18. This produces clock input signal 20 (CIN), inverted clock input signal (CIN') 21 and clock delay signal 22 (CDLY). Clock delay signal 22 is delayed by an ~~IO~~ I/O system delay t_{mdl} illustrated by block 24. CDLY 22 is also directly fed via line 23 into the SMD 12.

Page 5, lines 15-18. Applicant further depicted this relationship in Fig. 1. *See Fig. 1.* As described and depicted, Applicant therefore respectfully asserts that the receiver and buffer 18 **can** have an input connected to an external clock signal X_{clk} 16 and an output connected to CIN, CIN', and CDLY. Nevertheless, Applicant amended Claim 19 to reflect that the input buffer 18 has one input "**for receiving**" the external clock signal X_{clk} 16 and an output "**related to**" CIN, CIN', and CDLY.

Regarding **lines 5-8**, the Examiner asserts that the limitation is unclear due to the antecedent basis problem discussed in Item Number 5 above. However, Applicant's above Remarks also apply equally here. More specifically, Applicant amended the Specification on

Page 6, lines 13, 16 to make explicit that which was implicit, namely, that the measurement delay line has a **measurement delay line input** and **measurement delay line output**, and that the variable delay line has a **variable delay line input** and **variable delay line output**. Thus, the limitation recited on lines 5-8 should now be clear to the Examiner.

Regarding **lines 12-16**, the Examiner asserts that the limitation is unclear due to the antecedent basis problem discussed in Item Number 5 above. However, Applicant's above Remarks also apply equally here. More specifically, and in full accord with the foregoing, one skilled in the art can readily match each term used in the claim with the element(s) shown in the drawings.

Regarding **line 12**, the Examiner asserts that the term "the signals" lacks antecedent basis, i.e., it is unclear to the Examiner to which signals they are referring. However, Applicant respectfully asserts that one skilled in the art would have understood to which "signals" Applicant originally referred. Nevertheless, Applicant has identified that "the signals" on line 12 refers to the "**CIN and CDLY**" signals in amended Claim 19. Applicant has provided ample support for this amendment throughout the Specification. *See, e.g., Page 3, lines 13-18* ("a phase detection and selection circuit includes a phase detector for receiving a clock input signal CIN and a clock delay signal CDLY") *and Page 7, lines 4-5* ("Phase detector 26 receives clock input signal 20 and clock delay signal 22").

Regarding **line 14**, the Examiner asserts that the term "the circuit" lacks antecedent basis. However, the Applicant respectfully directs the Examiner to the preamble of this claim, whereby the Examiner may now see that the term "the circuit" has antecedent basis. Nevertheless, Applicant has identified that "the circuit" on line 14 is "a circuit" in amended Claim 19.

Also regarding **Claim 19**, the Examiner further asserts that the claim is incomplete since it does not have a logical structural relationship between recited elements. However, Applicant respectfully directs the Examiner to the language of the claim, to wit, "a phase detector **disposed between** the input buffer and the ~~synchronous mirror delay~~ SMD," *Claim 19, line 9 (emphasis added),* whereby Applicant has **not** merely listed elements without any recitation to particularly point out a relationship between elements, as the Examiner asserted. Applicant has provided ample support for this amendment throughout the Specification. *See, e.g., Page 4, lines 1-2* ("**interposing** a phase detector and selection system **between** an external clock signal and a synchronous mirror delay circuit") *(emphasis added)*; *Page 10, lines 8-9* ("a phase detector is

interposed between the synchronous mirror delay and CIN and CDLY signals") *(emphasis added)*; *Fig. 1; and Fig. 6, Step 74.*

Regarding **Claims 20-22**, the Examiner asserts that these claims are indefinite because of the indefiniteness of Claim 19. However, the above Remarks also apply equally here, whereby the Examiner's comments are rendered moot as per amended Claim 19 and the foregoing. More specifically, Applicant asserts that Claim 19 is not indefinite, and consequently, neither are dependent Claims 20-22.

Regarding **Claim 26**, the Examiner asserts that the recitation that the phase detector receives the inverted clock input signal is misdescriptive because as shown in Fig. 1, the CIN' signal is not received by the phase detector 26. However, Applicant amended Claim 26 to reflect that the phase detector 26 receives CIN and CDLY signals, but not CIN', whereby the phase detection and selection system selectively feeds CIN or CIN' into the SMD 12.

Also regarding **Claim 26**, the Examiner further asserts that the claim is incomplete because the recited function of "selectively feeding CIN and CIN' into the SMD" 12 is not supported by the recited elements, i.e., none of the recited elements supports the recited function. However, Applicant fails to understand the Examiner's assertions, as it is precisely the recited elements of the "phase detection and selection system" that supports the recited function of "selectively feeding CIN or CIN' into the SMD". Moreover, Applicant has provided ample support for this claim throughout the Specification. *See, e.g., Page 3, lines 19-21* ("when $t_{mdl} > t_{ck}/2$, CIN is input into the SMD, and when $t_{mdl} < t_{ck}/2$, an inverted clock signal CIN' is input into the SMD..."); *Page 5, lines 22-24* ("Ultimately, the phase of the signals will determine whether CIN 20 or CIN' 21 is used as the input to the SMD, or whether the SMD is bypassed altogether"); *and Page 5, line 25 through Page 6, line 12*:

> [A]ny suitable control logic may be used to define the conditions of the signals and select them accordingly. Associated with the phase detector is a multiplexor 28 which is used as an input selection multiplexor, that is to determine which selection input (CIN or CIN'), based on the difference between CIN signal 20 and CDLY signal 22, to send to the SMD 12. The outputs (collectively 32) of phase detector 26, which will be described in further detail with respect to ~~Fig. 2.~~ Fig. 2, are fed into circuitry control block 30. Circuitry block 30 may be, for instance, a decoder, although any suitable logic is contemplated. The outputs 38 and 40 of phase detection circuitry block 30 will be used to select the outputs for multiplexors 28 and 46, respectively. Based on the signal 38 from

> control circuitry block 30, input multiplexor 28 will select either CIN 20 or CIN' 21 to be placed on line 48. The output multiplexor 46 is used in combination with the control circuitry block 30 to select which signal is to be put on output line 50. Line 48 (either CIN signal 20 or CIN' signal 21) is directed into the SMD 12. Line 48 is also directed via connection 34 to an input of output selection multiplexor 46.

Finally, regarding **Claims 27-30**, the Examiner asserts that these claims are indefinite because of the indefiniteness of Claim 19. However, Applicant will assume that the Examiner intended to basis the Examiner's rejection of Claims 27-30 on the alleged indefiniteness of **Claim 26** (not Claim 19), as Claims 27-30 depend only from **Claim 26** (not Claim 19). Regardless, the above Remarks also apply equally here, whereby the Examiner's comments are rendered moot as per amended Claim 26 and the foregoing. More specifically, Applicant asserts that Claims 26 is not indefinite, and consequently, neither are dependent Claims 27-30.

Earnestly believing that Applicant has overcome all the 35 U.S.C. § 112 rejections to Claims 19-22 and 26-30, Applicant respectfully requests reconsideration and allowance of the same.

7. The Examiner rejected Claims 1-11, 13-30, and 34 under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,166,990 ("Ooishi").

Ooishi synchronizes internal and external clock signals by phase-locking an internal clock signal with an external clock signal. However, Ooishi fails to do so in a way that anticipates Applicant's inventive arrangements. For example, Fig. 40 presents a high-level view of Ooishi, in which it can be seen that a clock reproduction circuit comprises a Frequency Determination Circuit 83 and a Fine Adjust Circuit 85. *See Fig. 40.* The Frequency Determination Circuit 83 accepts four inputs (an output clock signal from a dummy delay circuit 81, a clock signal from a buffer circuit 82, TUP, and TDWN) and provides one output (clock output at node B). The Fine Adjust Circuit 85 accepts three inputs (clock input at node C, clock input at node D, and clock input at node E) and provides three outputs (clock output at node F, TUP, and TDWN).

Now regarding **Claim 13**, the Examiner asserts that Ooishi discloses a SMD circuit and phase detector connected thereto. To support this assertion, the Examiner refers to Fig. 39 and suggests that the Frequency Determination Circuit 83 is a SMD and that the Fine Adjustment Circuit 85 is a phase detector. Analyzing Ooishi, however, compels different conclusions.

More specifically, Ooishi depicts component 4 in Figs. 1, 9, 11-13, 22, 24-25, and 52 as a SMD, whereby it is not clear why the Examiner has declared that component 83 in Fig. 39 is also a SMD. Rather, Ooishi's synchronizing clock generation circuit 4 comprises a SMD 4b. *See, e.g., Column 14, lines 64-64 and Fig. 9.* Solving related problems (but in different ways), Ooishi notes "By using SMD 4b...an internal clock signal is generated in synchronization with the rise and fall of an external clock signal...". *Column 15, lines 52-55.* Regardless, Ooishi identifies component 83 as a Frequency Determination Circuit, and notes that it compares the phases of the clock signal from the dummy delay circuit 81 and buffer circuit 82. *See, e.g., Column 34, lines 28-31, Fig. 37, and Fig. 39.* Applicant's SMD 12, on the other hand, does not compare clock signals, but is instead fed i) CDLY 22 via line 23 and ii) either CIN or CIN'. *See, e.g., Page 5, lines 15, 23.* In any event, Ooishi's Frequency Determination Circuit 83 is pragmatically different than Applicant's SMD 12.

Similarly, Ooishi depicts component 60 in Figs. 27-28 as a phase compurgator (and component 100 in Figs. 43, 59 as a phase comparison circuit 100), whereby it is not clear why the Examiner has declared that component 85 in Fig. 39 is also a phase detector. However, while Applicant acknowledges that the Fine Adjust Circuit 85 depicted in Fig. 43 includes the "phase comparison circuit" 100, Ooishi does not suggest these components are synonyms, interchangeable, or otherwise without distinction. But Even if Ooishi's Fine Adjust Circuit 85 can be deemed a phase detector, it does not input CIN or CIN' into a SMD. Rather, it inputs TUP or TDWN into the Frequency Determination Circuit 83, as will be presently elaborated upon.

The Frequency Adjust Circuit 85 adjusts the phase of clock output at node F (CLKf) according to a phase comparison analysis between the clock signal from the replica buffer 88 at node E and the reference clock signal RFCK at node D. *See, e.g., Column 34, lines 40-44; Column 35, lines 20-23; Fig. 37; and Fig. 39.* However, the clock signal from the replica buffer 88 is fed into the Frequency Adjust Circuit 85 directly from the Clock Tree 87 at node A. Applicant, on the other hand, does not directly feed outputs from the Applicant's Clock Tree 54 into Applicant's Phase Detector 26. Rather, Applicant compares CIN with CDLY, the CDLY being a clock delay signal 22 delayed by an I/O system delay t_{mdl}. *See, e.g., Page 5, line 17.*

Moreover, as shown in Fig. 39, Ooishi sets a first delay time La equal to a second delay time Lb. *See Column 35, line 12.* Thereafter, the Fine Adjust Circuit 85 sets the phase of the

clock signal at node D to be the same as the phase of the clock signal at Node E. *See Column 36, lines 3-5.* In other words, Ooishi's Fine Adjust Circuit 85 sets the phase difference of the clock signals applied at input nodes D and E to **zero**. *See Column 35, lines 64-65.* The Fine Adjust Circuit 85 does this so that "the phase of clock signal intCLK at node A can be made equal to the phase of clock signal eCLK at clock input pad 75a." *Column 36, lines 5-7.*

Stated differently, the Fine Adjust Circuit 85 adjusts the phase of the output clock signal CLKf according to the external clock signal eCLK so that the clock signal CLKo from node B can be made to properly synchronize in phase with the external clock signal eCLK according to the signals TUP and TDWN. *See Id. at 11-18.* To accomplish the foregoing, Ooishi discloses that when the phase of the clock signal of node D **lags behind** the phase of the clock signal of node E, TUP *increases* the delay time of the Frequency Determination Circuit 83 by one delay stage (in each delay chain). *See, e.g., Column 38, lines 23-24 and Column 39, lines 5-11.* Similarly, when the phase of the clock signal of node D is **ahead** of the phase of the clock signal of node E, TDWN *decreases* the delay time of the Frequency Determination Circuit 83 by one delay stage (in each delay chain). TUP and TDWN thus adjust the output of the Frequency Determination Circuit 83 until the inputs at nodes D and E are synchronized. Unlike Applicant's components, **both** the Frequency Determination Circuit 83 **and** Fine Adjustment Circuit 85 compare phases of various clock signals, working together to accomplish synchronization, speeding up and slowing down a delay period as necessary. *See also Column 38, lines 27-30* ("When the difference in phase of the clock signal is greater than delay time TD (when the fine adjust range is exceeded), the delay time of frequency determination circuit 83 is adjusted"); *Column 44, line 63 through Column 45, line 3* ("Since the delay time of the fine adjust circuit corresponds to a delay time of one delay stage of the coarse adjust circuit and the delay stage of the coarse adjust circuit is shifted by one stage when the adjustment range of the fine adjust circuit is exceeded, an internal clock signal can be locked in phase with an external clock signal at high precision and high speed"); and *Column 66, lines 16-45* ("When internal clock signal CLKI is ahead in phase of external clock signal CLKI shown in FIG. 78, phase comparator PC continuously renders signal NFA active...When the timing of input clock signal CLKI lags behind external clock signal CLKE, phase comparator TC renders signal NSL active").

Finally, Ooishi discloses that a period of **two** clock cycles of an internal clock signal CLKi is a typical lock period. *See, e.g., Column 15, lines 25-26 and Fig. 10. See also Column*

25, lines 7-8 ("[the] clock signal CLKd from clock driver 56 is delayed by 2 clock cycles"). Under the disclosed conditions, Applicant however, inter alia, reduces the delay length from 2 clock cycles to **1 clock cycle** by selectively inputting CIN or CIN' into the SMD, and altogether bypasses the SMD 12 while selectively inputting CIN or CIN' directly into the clock tree.

In accordance with the foregoing, Ooishi fails to disclose Applicant's inventive arrangements, including reducing a number of effective delay stages in the SMD. More specifically, and as previously discussed, Applicant has disclosed and claimed that two signal branches 32, 34 yield one of a maximum of four possible combinations, namely (0,0), (0,1), (1,0), or (1,1). If the output of the phase detector 26 is **(0,0)**, CIN is input into the SMD 12 and then into the Clock Tree 54 via SMDOUT. If the output of the phase detector 26 is **(1,1)**, CIN' is input into the SMD 12 and then into the Clock Tree 54 via SMDOUT. If the output of the phase detector 26 is **(1,0)**, CIN is input directly into the Clock Tree 54, *bypassing* the SMD 12 and SMDOUT. Finally, if the output of the phase detector 26 is **(0,1)**, CIN' is input directly into the Clock Tree 54, *bypassing* the SMD 12 and SMDOUT. Accordingly, Ooishi fails to disclose "the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality of conditions of the clock input signal and the clock delay signal based on the timing characteristics, and wherein at least one of the conditions reduces a number of effective delay stages in the SMD." The Examiner's reference to *Column 38, lines 32-35* is misguided in so far as Ooishi's reference to a coarse adjustment circuit working in conjunction with a fine adjustment circuit to reduce the number of delay stages in the latter does not anticipate interposing a phase detector before a SMD in order to, inter alia, reduce the delay length from 2 clock cycles to 1 clock cycle by selectively inputting CIN or CIN' into the SMD, or altogether *bypassing* the SMD 12 while selectively inputting CIN or CIN' directly into the clock tree.

Earnestly believing Claim 13 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 14**, the Examiner asserts that the recited limitation is merely the definition of the clock input signal CIN, and since the Ooishi's clock input signal RFCK can be defined as recited, the recited limitation is met. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Applicant respectfully directs the Examiner to the entirety of the language of the claim, in which Applicant has identified the four phases/conditions that can detected by the phase detector 26, whereas Ooishi fails to disclose or teach these phases/conditions. Therefore, the recited results will not—and cannot—be met by Ooishi. Earnestly believing Claim 14 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claims 15-17**, the Examiner asserts that the recited limitations are merely the results when the Ooishi circuit operates, i.e., the TUP and TDWN signals control the number of effective delay stages in the SMD. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi discloses component 102 as a bi-directional shift register and component 106 as a decision circuit, whereby Ooishi uses the TUP and TDWN to respectively increase and decrease the delay time of the Frequency Determination Circuit 83 until the inputs at nodes D and E are synchronized. Applicant, on the other hand, is not increasing and decreasing *a delay period* to achieve synchronization, but *cutting the entire delay period* to achieve faster synchronizations under specified conditions. Therefore, the recited results will not—and cannot—be met when the Ooishi circuit operates. Earnestly believing Claims 15-17 therefore recite patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 18**, the Examiner repeats the rejection stated in the rejection of Claims 13 and 14 and asserts that the limitations recited on lines 16-17 are met since it is merely the result when the circuit operates, i.e., by reducing the number of effective delay stages in the second phase and by bypassing the SMD in the third and forth phases, the optimum phase latching time is achieved by Ooishi's circuit. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Applicant respectfully directs the Examiner to the entirety of the language of the claim, in which Applicant

has identified the four phases/conditions that can be detected by the phase detector 26, whereas Ooishi fails to disclose or teach these phases/conditions. Since Ooishi fails to disclose or teach these phases/conditions, Ooishi does not—and cannot—disclose reducing the number of effective delay stages in the second phase and bypassing the SMD in the third and forth phases. At a minimum, Ooishi does not—and cannot—disclose bypassing the SMD. Earnestly believing Claim 18 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 19**, the Examiner objected to the Examiner's best guesses while preserving the right to assert new grounds of rejections if necessitated by Applicant changes to said claim. However, the Examiner's comments are rendered moot as per amended Claim 19 and the foregoing. Regardless, Applicant respectfully traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, the Examiner notes that the input buffer is "not shown," yet claims Ooishi *anticipates* Applicant's claim containing such a component. Applicant is at a loss and seeks clarification. Applicant is also at a loss regarding the Examiner's references to Ooishi's measurement delay line, measurement delay line input, measurement delay line output, variable delay line, variable delay line input, and variable delay line output—and seeks clarification from the Examiner regarding Ooishi's use thereof. In the meantime, earnestly believing Claim 19 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claims 20-22**, the Examiner rejected these claims for the same reasons noted in Claims 15-18. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi does not disclose inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ and inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$. Ooishi also does not disclose reducing the number of effective delay stages in the SMD when $t_{mdl} < t_{ck}/2$. Ooishi also does not disclose reducing the number of effective delay stages in the SMD from 128 to substantially 59 when $t_{mdl} < t_{ck}/2$. Earnestly believing Claims 20-22 therefore recite patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 23**, the Examiner rejected this claim for the same reason noted in Claim 18. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi fails to disclose "the phase detector outputting a pair of branches each having a logical level, wherein the logical levels of the branches define a plurality based on the timing characteristics, and wherein a number of effective delay stages of the SMD is reduced." Earnestly believing Claim 23 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 24**, the Examiner asserts that the recited condition is met when Ooishi's SMD operates. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi fails to disclose or teach the phases/conditions that can detected by the phase detector 26, yet alone that under one condition, the number of effective delay stages is reduced by substantially one-half. Therefore, the recited condition will not—and cannot—be met when Ooishi operates. Earnestly believing Claim 24 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 25**, the Examiner rejected this claim for the same reason noted in Claim 18. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Applicant respectfully directs the Examiner to the entirety of the language of the claim, in which Applicant has identified the four phases/conditions that can detected by the phase detector 26, whereas Ooishi fails to disclose or teach these phases/conditions. Since Ooishi fails to disclose or teach these phases/conditions, Ooishi does not—and cannot—disclose reducing the number of effective delay stages in the second phase. Earnestly believing Claim 25 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 26**, the Examiner rejected this claim for the same reason noted in Claim 13, and asserts that i) the recited logic reads on the circuits 102 and 106 shown in Fig. 43; ii) the recited limitations on the last three lines are met since they merely recite the operation of the circuit; and iii) the recited CIN reads on ECLK clock and the recited CIN' reads on the not(ECLK) clock. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi discloses component 102 as a bi-directional shift register and component 106 as a decision circuit,

whereby the recited logic of "select[ing] one of the output signal combinations corresponding to the timing conditions of the signals" cannot be anticipated by Ooishi's bi-directional shift register 102 and decision circuit 106, the latter of which apparently directs TUP and TDWN, but otherwise does not select one of the plurality of output signal combinations. In addition, the recitation "upon which the plurality of output signal combinations is generated and wherein a number of effective delay stages is reduced" does not recite the operation of the circuit, as asserted by the Examiner in reference to the last three lines of the claim, since the operation of the circuit does not generate a plurality of output signals to reduce a number of effective delay stages. Earnestly believing Claim 26 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claims 27-30**, the Examiner rejected these claims for the same reasons noted in Claims 14-17 respectively. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Applicant respectfully directs the Examiner to the entirety of the language of the claim, in which Applicant has identified the four phases/conditions that can detected by the phase detector 26, whereas Ooishi fails to disclose or teach these phases/conditions. Therefore, the recited results will not—and cannot—be met by Ooishi. Earnestly believing Claims 27-30 therefore recite patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claim 34**, the Examiner rejected this claim for the same reasons noted in Claim 13, and asserts further that i) the limitations recited on lines 2-7 are merely standard features in a computer system; ii) since the Ooishi circuit shown in Fig. 1 is for a memory circuit in a computer system, the recited limitations are met; iii) the recited logic reads on the circuits 102 and 106 shown in Fig. 43; iv) the recited limitations on the last four lines are met since they merely recite the definition of the clock input signal CIN and the operation of the circuit. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi discloses component 102 as a bi-directional shift register and component 106 as a decision circuit, whereby the recited logic of "select[ing] one of the output signal combinations corresponding to the timing conditions of the signals" is not anticipated by Ooishi's bi-directional shift register 102 and decision circuit 106, the latter of which apparently directs TUP and TDWN, but otherwise does not select one of a plurality of output signal combinations. In addition, the

recitation "inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ reduces a number of delays stages in the SMD" does not recite the operation of the circuit, as asserted by the Examiner in reference to the last four lines of the claim, since the operation of the circuit does not input CIN into the SMD when $t_{mdl} > t_{ck}/2$ and input CIN' into the SMD when $t_{mdl} < t_{ck}/2$. Earnestly believing Claim 34 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

As per **Claim 1**, the Examiner asserts this claim is merely a method to operate a SMD circuit having elements and connections shown in Fig. 39, and since Ooishi teaches the circuit as discussed in detail in Claim 18 above, Ooishi inherently teaches the recited steps. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, selectively inputting CIN or CIN' into the SMD based on the phase of CIN and CDLY to reduce a number of required delay stages in the SMD is not the result of operating a SMD circuit having elements and connections shown in Fig. 39, since operating a SMD circuit having those elements and connections will not—and cannot—achieve these results. Moreover, since Ooishi does not teach the circuit discussed in detail in Claim 18 above, for the reasons identified there, Ooishi does not—and cannot—teach the recited steps. Earnestly believing Claim 1 therefore recites patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Incidentally, the Examiner's note "A comprehensive steps are further disclosed when reading the operation of the circuit shown in Fig. 39" is either a typo or unintelligible. If the Examiner deems it relevant, Applicant respectfully seeks clarification.

Regarding **Claims 2-4**, the Examiner asserts these claims are discussed in Claims 14, 16, and 17, respectively. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi does not disclose inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduce the number of required delay stages in the SMD. Therefore, the recited method step will not—and cannot—be met by Ooishi. Earnestly believing Claims 2-4 therefore recite patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Regarding **Claims 5-11**, the Examiner rejected these claims for the same reasons noted in Claims 34, 34, 18, 14, 34, 34, and 14, respectively. Respectfully, Applicant traverses and requests withdrawal.

Applicant's above Remarks also apply equally here. More specifically, Ooishi fails to interpose a phase detector and selection system between an external clock signal and a SMD circuit, determine which of a number of phases the signals are in based on the timing characteristics, or selectively direct the signals based upon the phase of the signals, as recited in **Claim 5**. In addition, Ooishi also fails to selectively direct CIN or CIN' to the SMD based upon the timing characteristics of CIN and CDLY, as recited in **Claim 6**. Furthermore, Ooishi also fails to disclose bypassing CIN or CIN' from the SMD based upon the timing characteristics of CIN and CDLY as recited in **Claim 7**. Moreover, Ooishi also fails to determine that the phases include one of four phase/conditions, as recited in **Claim 8**. Yet further, Ooishi also fails to select one of CIN and CIN' to be input into SMD, thereby reducing the effective delay stages in the SMD, as recited in **Claim 9**. Further yet still, Ooishi also fails to direct CIN' into the SMD such that a reduced number of delay stages are achieved, as recited in **Claim 10**. Finally, Ooishi also fails to direct CIN' into the SMD when $t_{mdl} < t_{ck}/2$, as recited in **Claim 11**. Therefore, the recited method steps will not—and cannot—be met by Ooishi. Earnestly believing Claims 5-11 therefore recite patentable subject matter, Applicant respectfully requests reconsideration and allowance of the same.

Earnestly believing that Applicant has overcome all the 35 U.S.C. § 102 rejections to Claims 1-11, 13-30, and 34, Applicant respectfully requests reconsideration and allowance of the same.

8. Regarding **Claim 12**, the Examiner objected to this claim as being dependent upon a rejected base claim, but indicated it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, for which Applicant is grateful. Accordingly, Applicant has rewritten Claim 12 in independent form including all of the limitations of the base claim and any intervening claims, and accordingly, respectfully requests reconsideration and allowance of the same.

9. The prior art made of record and not relied upon is acknowledged. Nothing in those references teaches or suggests Applicant's inventive arrangements as claimed.

CONCLUSION

Applicant discloses and claims a phase detection system and method for use with a SMD. The invention takes a clock input signal and a clock delay signal, each having timing characteristics, and differentiates between **four** conditions based upon timing characteristics of the signals. Each of the four conditions are exclusive, and one must be true. A phase detector determines, based upon the timing characteristics of the signals, which condition the signals are in. Selectors select the signals to be introduced into the SMD based upon the timing characteristics of the phase conditions. The invention utilizes the falling clock edge of the clock input signal and decreases lock time under specific phase conditions. The invention increases efficiency of circuits by reducing effective delay stages in the SMD.

Ooishi fails to teach all of the claimed limitations of Applicant's inventive arrangements. In any event, Applicant believes this Response overcomes all of the Examiner's rejections and objections. Thus, Applicant believes the Examiner cannot establish or maintain proper rejections or objections to the Specification or claims. Accordingly, Applicant respectfully requests withdrawal of all rejections and objections.

Applicant believes this Response should allow the Examiner to allow the above-referenced patent application to issue as a U.S. patent without further amendments to the Specification or claims. Applicant respectfully submits that all pending claims are in condition for allowance, which Applicant requests. Applicant also solicits notification to that effect. However, if any questions should arise, Applicant hereby encourages the Examiner to telephone the undersigned attorney.

EXTENSION OF TERM

The proceedings herein are for a patent application, and the provisions of 37 CFR § 1.136 apply. Applicant believes this Response requires a one-month extension of time, which Applicant hereby requests. However, Applicant also makes this conditional petition in case Applicant inadvertently overlooked the need to petition for a different extension of time, in which case Applicant hereby requests if applicable. In any event, the Examiner is hereby authorized to charge any amounts due and owing to Deposit Account 232053.

Respectfully submitted,

Dated: 5/2/03

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